Modeling of Drain Current for Grooved-Gate MOSFET

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A drain current model of grooved-gate MOSFET, which is based on the difference of the channel depth distance along the channel from the source to the drain in cylindrical coordinate system, is presented in this paper. From the analysis, the potential of grooved-gate is related to geometry structure parameters, the angle (θ_0) and the radius (r_0) of concave corner, as well as the channel depth (d). The presence of corner effect will influence the drain potential, drain current characteristics, and the other electrical characteristics, such as conductance (g_m) and transconductance (g_d). In this result, our model shows the effect of corner along with an improvement in the device characteristics. In particular, the reduction of short channel effect (SCE) is shown. However, the drain current value of the grooved-gate MOSFET is slightly less than that of the ordinary MOSFET.

Keywords: grooved-gate MOSFET, curved channel, drain current model, Short Channel Effect (SCE), potential barrier.

1. INTRODUCTION

The small geometry of conventional bulk silicon MOSFETs into the nanoscale regime has many problems associated with short-channel effects (SCEs). The grooved-gate MOSFET, which is created by corner region, offers a promising structure to reduce the Short Channel Effect. The influence of the corner effect may affect the potential barriers for the device channel [1-3] which can improve the characteristics of the device. Such improvement includes the reduction of short channel effect (SCE) such as a high threshold voltage roll-off (V_{th}), a low DIBL and GIDL effect, closeness to ideal sub-threshold slope, and a high I_{ON}–I_{OFF} ratio [1-7]. An analytical numerical model of surface potential on Grooved-Gate MOSFET has been made using the 2D

Poisson equation method in cylindrical coordinates [l] in which the potential distribution function along channel, $V(\theta)$, relates to the grooved-gate MOSFET structural parameters (r_0, θ_0, and d), substrate doping and applied biases.

In this paper, we present a new drain current model for drain current characteristics of grooved-gate MOSFET, based on a determination of channel depth at its respective angle in the cylindrical coordinate system. The model is an approximation of the geometrical structure in the cylindrical coordinate system. It has a curved region geometry which is capable of accurately simulating the I-V characteristics of grooved-gate MOSFET. The dependence of I-V characteristics on corner radius (r_0), corner angle (θ_0), channel depth (d), channel length (L) is shown in the paper.

2. DEVICE STRUCTURES AND SIMULATION

The grooved-gate MOSFET structure with depletion region is shown in Fig. 1. The gate electrode of device is located on a groove region separating the source and drain regions. In order to form the effective minus junction depth, the junctions of source/drain are made shallower than the groove bottom.

The presence of the groove in grooved-gate MOSFETs can enhance the electrical performance [8]. The curved structure at the channel of device is effective in reducing the electric field at the drain. Furthermore, it can also reduce the substrate current, and increase the voltage from gate to drain, thus improving the reliability of the device.

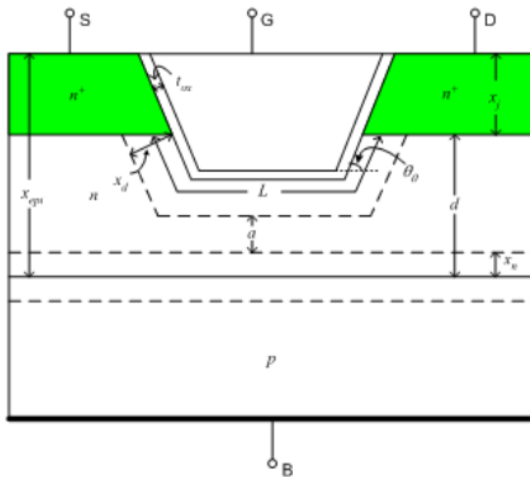

Figure 1: The Grooved-gate MOSFET structure

There are several geometrical parameters include in groove-gate MOSFETs such as channel length (L), junction depth (x_j), the angle of the vertical concave sidewall structure (θ_0), and depletion depths of gate (x_d) and substrate (x_n). These parameters can influence drain current value and others electrical performance, such as sub-threshold swing (S), minimum surface potential, DIBL and threshold voltage roll-off, etc.

3. MODEL OF DEVICE STRUCTURE

The grooved-gate structure of device can be approximated as the concave corner which is part of cylinder [1]. This device is shown in Fig. 2 below.

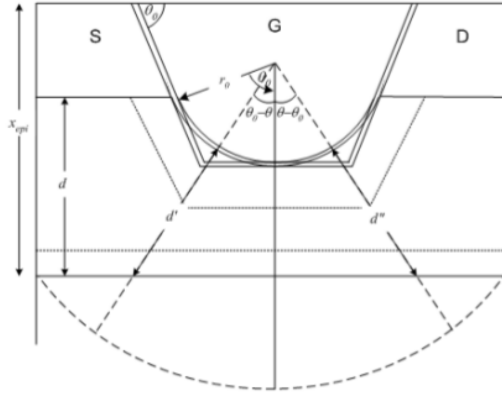

Figure 2: The Grooved-gate MOSFET with cylindrical approximation of concave corner

The variation of the parameters, such as the concave corner radius (r_0), junction depth (x_j), the angle of the concave gate structure (θ_0) and the channel doping concentration can improve the performance and the short-channel effect (SCE). The electron potential profile in the channel region having concave corner, is derived by the Poisson equation in the cylindrical coordinates. The potential distribution function along the channel from analytical model solution [1] has been derived as :

$$V(\theta) = V_{BS} - \frac{M}{2x_{deff}}(V_g - \varphi_s(\theta))(R_2 - r)^2 \qquad (1)$$

Where M and x_{deff} are constant, $M = \frac{C_{oxc}}{\varepsilon_{Si}}$ and $x_{deff} = \sqrt{\frac{2\varepsilon_{Si}}{qN_A}1.5V_{bi}}$, respectively, and C_{oxc} is the gate oxide capacitance per unit area [1] of the corner region of the groove gate, with $C_{oxc} = \frac{\varepsilon_o \varepsilon_{ox}}{r_0 \ln\left(1 + t_{ox}/r_0\right)}$

The modification of the potential equation at (1) using derivation of Poisson equation (as shown at Appendix A) and assumption of the potential equation $V(\theta)$ at surface is surface potential $\varphi_s(\theta)$, we obtain :

$$V(\theta)=\frac{1}{Sinh\left(\frac{2\theta_0}{\lambda}\right)}\left[(\Phi_s+V_d)\,Sinh\left(\frac{\theta}{\lambda}\right)+\Phi_s Sinh\left(\frac{2\theta_0-\theta}{\lambda}\right)\right]+\zeta \quad (2)$$

where λ and ζ are constants, $\lambda = x_{deff}\sqrt{\frac{2}{x_{deff}-R_1}}$ and $\zeta = V_g - \frac{N_A q x_d R_1}{C_{oxc}(x_d - R_1)}$, respectively.

4. MODEL OF I-V CHARACTERISTICS

The equation of the I-V characteristics based on the difference of channel depth distance of the device is given by [10]:

$$I_d R_1 d\theta = N_D q \mu_{eff} W a(\theta) dV(\theta) \quad (3)$$

where W is the channel width, μ_{eff} is the effective electron mobility, $V(\theta)$ is the potential in the channel in the radial direction at angle θ, and $a(\theta)$ is the effective channel depth distance along the channel from the source to the drain and is given by:

$$a(\theta) = d' - x_n(\theta) - x_d(\theta) \quad (4)$$

where d' is the effective channel depth, x_d and x_n are the depths of depletion regions of the gate and the substrate respectively. This potential is zero at the source ($\theta = 0$), and it is the value of V_d at the drain ($\theta = 2\theta_0$).

The depth of the depletion region of the gate, x_d , is given by [9]:

$$x_d = \frac{\varepsilon_{Si}}{2C_{ox}}\left((1+\delta(V_g - V(\theta)))^{1/2} - 1\right) \quad (5)$$

where δ is constant, $\delta = -\frac{2C_{oxc}^2}{\varepsilon_{Si} q N_D}$, N_D is the channel doping, θ is the electronic charge, and ε_{Si} is the permittivity of silicon.

The depth of depletion region of the substrate, x_n , is given by :

$$x_n = K_o\left(\phi_{bi} + V_B + V(\theta)\right)^{1/2} \quad (6)$$

where K_o is constant, $K_o = \left(\frac{2\varepsilon_{Si} N_A}{q N_D (N_A + N_D)} \right)^{1/2}$, ϕ_{bi} = (kT/q) ln $(N_A N_D / n_i^2)$ is the built-in potential, V_B is the substrate voltage, N_A and N_D are the acceptor and donor concentrations, respectively.

5. I_d-V_d CHARACTERISTICS

From Fig. 2, the distance d between the bottom of the groove and the p-n junction of the source/drain boundary is :

$$d = x_{epi} - x_j \tag{7}$$

where x_{epi} is the thickness of the epitaxial layer and x_j is the junction depth of the source/drain n+ diffusion.

The determination of effective channel depth distance is separate being two calculations due to the geometry of distance $a(\theta)$ will increase from source to middle of channel and will decrease from middle of channel to drain as given by:

$$a(\theta) = \begin{cases} a'(\theta) = d' - x_d(\theta) - x_n(\theta) & 0 < \theta < \theta_0 \quad (8) \\ a''(\theta) = d'' - x_d(\theta) - x_n(\theta) & \theta_0 < \theta < 2\theta_0 \quad (9) \end{cases}$$

where :

$d' = d\ Sec(\theta_0 - \theta) - R_1 Cos(\theta_0) Sec(\theta_0 - \theta) - R_1$, and
$d'' = d\ Sec(\theta - \theta_0) - R_1 Cos(\theta_0) Sec(\theta - \theta_0) - R_1$

The calculation of d' and d'' can be seen at Appendix B.

The integration of drain current from eq (3) given as

$$I_d = \frac{N_D q \mu_n W}{2 R_1 \theta_0} \left[\int_{V(\theta=0)}^{V(\theta=\theta_0)} a'(\theta) dV(\theta) + \int_{V(\theta=\theta_0)}^{V(\theta=2\theta_0)} a''(\theta) dV(\theta) \right] \tag{10}$$

From the above integration, we obtain the I_d-V_d equation given as :

$$I_d = \frac{N_D q \mu_{eff} W}{2 R_1 \theta_0} \left[\frac{V_d \theta_0}{2\lambda} \left(d - R_1 Cos(\theta_0) \right) Csch\left(\frac{\theta_0}{\lambda} \right) \right.$$

$$+\frac{\theta_0}{\lambda}Csch\left(\frac{2\theta_0}{\lambda}\right)(dSec(\theta_0)-R_1)\left((\phi_{SG}+V_d)Cosh\left(\frac{2\theta_0}{\lambda}\right)-\phi_{SG}\right)$$

$$-R_1V_d+\frac{V_d\varepsilon_{Si}}{C_{ox}}+\frac{\varepsilon_{Si}}{3C_{ox}\delta}\left(1-(V_d+\phi_{SG}-V_g)\delta\right)^{3/2}-\frac{2}{3}K_0(V_d+\phi_{SG}+V_B+\phi_{bi})^{3/2}$$

$$-\frac{\varepsilon_{Si}}{3C_{ox}\delta}\left(1-(\phi_{SG}-V_g)\delta\right)^{3/2}+\frac{2}{3}K_0(\phi_{SG}+V_B+\phi_{bi})^{3/2}\Bigg] \quad (11)$$

where ε_{Si}, ε_0 are the permittivities of silicon and silicon dioxide respectively and t_{ox} is the oxide thickness along the walls of the groove, V_d is the drain voltage, and V_g is the effective gate voltage. The parameters K_o and δ are the constants defined above.

The source-drain conductance g_d is the differentiation of I_d with respect to V_d and is given by:

$$g_d=\left.\frac{dI_d}{dV_d}\right|_{V_d=0}=\frac{N_DqW\mu_{eff}}{2R_1\theta_0}\Bigg(R_1+\frac{\varepsilon_{Si}}{C_{ox}}-K_o\sqrt{V_{bs}-V_g+\phi_{bi}+\phi_{SG}}-\frac{\varepsilon_{Si}}{2C_{ox}}\sqrt{1-\delta(\phi_{SG}-V_g)}$$

$$+\frac{\theta_0}{2\lambda}\left(d-R_1Cos(\theta_0)\right)Csch\left(\frac{\theta_0}{\lambda}\right)+\frac{\theta_0}{\lambda}\left(dSec(\theta_0)-R_1\right)Coth\left(\frac{2\theta_0}{\lambda}\right)\Bigg) \quad (12)$$

The transconductance g_m in the saturation region is the differentiation of I_d with respect to V_g in the saturation region:

$$g_m=\left.\frac{dI_d}{dV_g}\right|_{V_d=V_{ds}}=\frac{N_DqW\mu_{eff}}{2R_1\theta_0}\Bigg(K_o\sqrt{V_{bs}+V_{ds}-V_g+\phi_{bi}+\phi_{SG}}-K_o\sqrt{V_{bs}-V_g+\phi_{bi}+\phi_{SG}}$$

$$-\frac{\varepsilon_{Si}}{2C_{ox}}\sqrt{1-\delta(\phi_{SG}-V_g)}+\frac{\varepsilon_{Si}}{2C_{ox}}\sqrt{1-\delta(V_{ds}+\phi_{SG}-V_g)}\Bigg) \quad (13)$$

6. RESULT AND DISCUSSION

The I_d-V_d characteristics can be obtained from equation (11) as shown in Fig. 3. This graph shows that the current drain reduction compared to the planar MOSFETs due to corner effect that effective in reducing the electric field. This also can decrease the substrate current, and increases the highest applicable gate to drain voltage, hence improving the reliability of the device. [3]

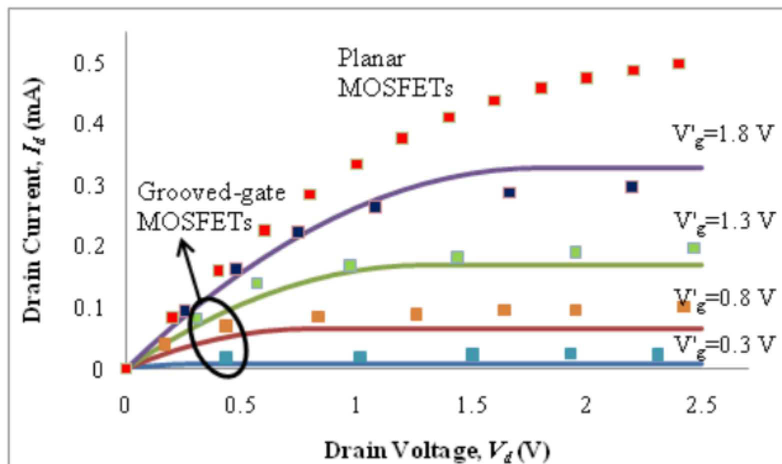

Figure 3: I_d-V_d Characteristics of Planar and Grooved-Gate MOSFETs, with θ_0=20°

and r_0=1.2 nm

Some researchers have demonstrated an improvement in the drive curent with some treatment. One of them is using a hydrogen anneal at 800 ◦C that gives a 30% improvement in the drive current at 120-nm n-channel transistors [10].

The drain current graphs of device with various concave corner angles are given in Fig. 4 and 5 for various θ_0 from 0° to 90°. The device with minimum angle of corner (0°) is like a planar device. These graphs show that the drain current decreases for a relatively larger corner angle.

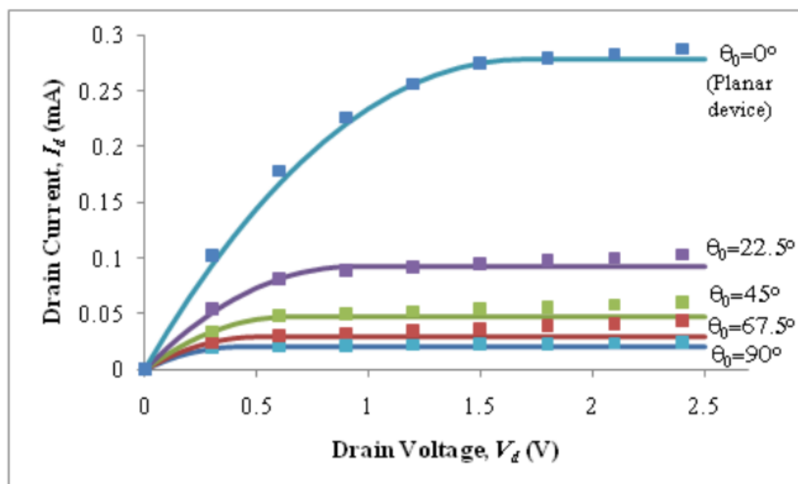

Figure 4: . I_d-V_d graphs with various θ_0 (0°-90°) and V_g=1.3 V.

In other words, the presence of the corner effects can reduce the drain current because the potential barrier for electron flow from source to drain will increase and then the potential barrier which is effective in suppressing the short channel effect degrades the drain current characteristics as compared to the planar device.

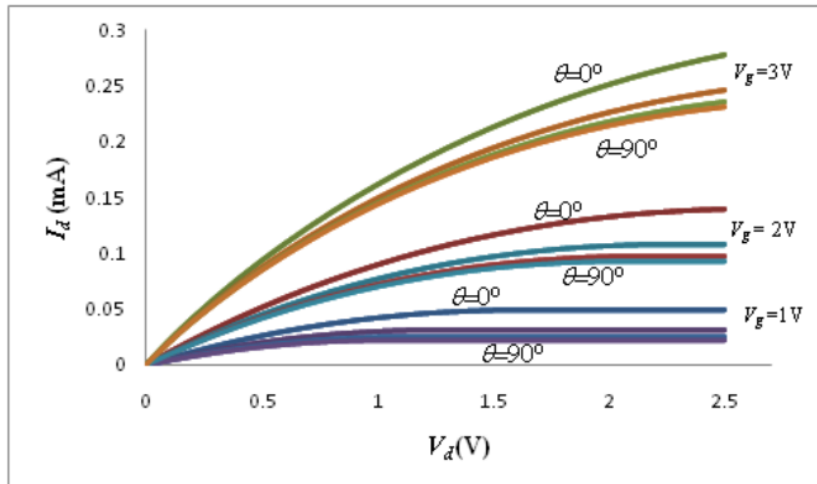

Figure 5: Id-Vd graphs with various θ_0(0°-90°) and V_g(1V-3V)

Figure 6 shows a typical set of I-V characteristic curves for the grooved-gate MOSFET geometry with various geometric channel depths *d*. The graph shows the drain current increase with a channel depth d increase for all gate voltage values. It means that for a device with the smaller *d*, it will be easy to compute MOS gate pinch-off and for higher *d*, the saturation of drain current does occur although the gate pinch-off may not occur.

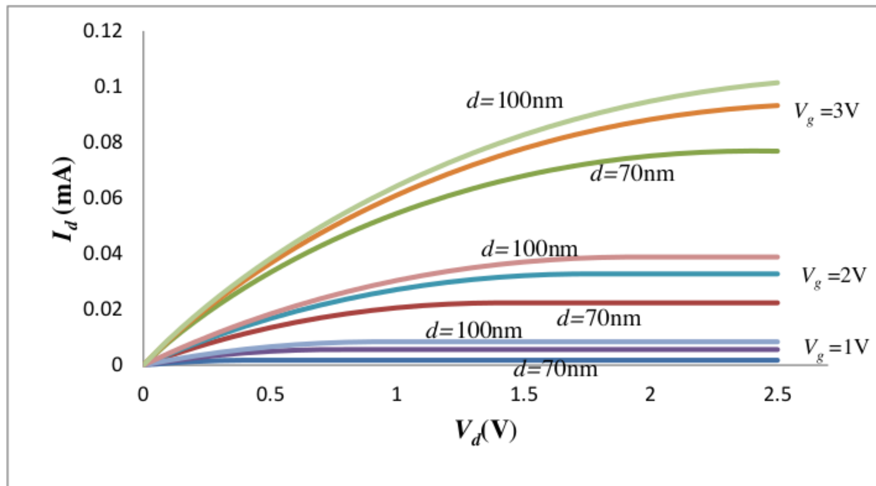

Figure 6: I_d-V_d Characteristics with various d(70nm-100nm) and V_g(1V-3V)

For the pinched-off devices, there are electrical characteristics measurements which include I-V characteristics, conductance below saturation, transconductance in the saturation region, pinch-off voltage and etc. For grooved-gate, the transconductance (g_m) and conductance (g_d) are very much correlated with device geometry, especially, the corner angle. The Figure 7 shows graphs of normalized transconductance (g_m) and conductance (g_d) with normalized angle of corner. The transconductance gm increases exponentially as the corner angle of device increases. In contrast with it, the conductance (g_d) decrease linearly when angle of corner increases.

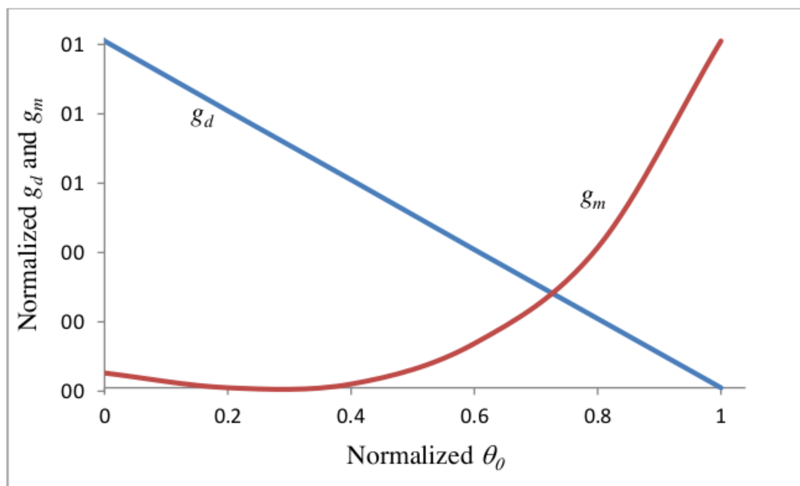

Figure 7: The graphs of normalized of conductance (g_d) and transconductance (g_m) of device as various normalized θ_0

These results are obtained directly from solving equations (12) and (13) instead of using the modulation of normalized θ_0 which assumes that the effective channel length decreases with drain voltage increases beyond saturation when pinch off does occur.

6. CONCLUSION

This drain current model of grooved-gate MOSFET is based on the channel depth distance along the channel using the 2D Poisson equation solution in the cylindrical coordinates. The structure includes some parameters, such as the concave corner radius, junction depth, the angle of the vertical concave sidewall structure and the channel doping concentration.

The result shows a reduction of the drain current due to the potential barrier from the implanted channel region and the curved structure. Furthermore, it is effective in reducing the electric field at the drain, thus improving reliability of short channel effects (SCEs), such as including sub-threshold swing (S), minimum surface potential, DIBL and threshold voltage roll-off, etc. For the drain current reduction, it has been done using experiment of a hydrogen anneal at 800 °C that gives a 30% improvement of the drive current for the device.

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