LEMBAR
HASIL PENILAIAN SEJAWAT SEBIDANG ATAU *PEER REVIEW*
KARYA ILMIAH : *PROSIDING* *

Judul Karya Ilmiah (Artikel)	:	Short Channel Effect of SOI Vertical Sidewall MOSFET		
Nama/Jumlah Penulis	:	**Jatmiko E. Suseno**, Munawar A. Riyadi, dan Razali Ismail (3)		
Status Pengusul	:	Penulis pertama/~~penulis ke.....~~ /~~penulis korespondensi **~~		
Identitas Makalah	:	a. Judul Prosiding	:	2008 IEEE International Conference on Semiconductor Electronics (ICSE 2008)
		b. ISBN/ISSN	:	978-1-4244-2560-0
		c. Tahun Terbit, Tempat Pelaksanaan	:	2009, Johor Bahru, Malaysia DOI:10.1109/SMELEC.2008.4770370
		d. Penerbit/Organiser	:	IEEE
		e. Alamat repository PT/web prosiding	:	https://ieeexplore.ieee.org/document/4770370
		f. Terindeks di (jika ada)	:	Scopus

Kategori Publikasi Jurnal Ilmiah (beri ✓pada kategori yang tepat) : ☑ *Prosiding* Forum Ilmiah Internasional
☐ Jurnal Ilmiah Nasional Terakreditasi

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b. Ruang lingkup dan kedalaman pembahasan (30%)	7,5		7.3
c. Kecukupan dan kemutahiran data/informasi dan metodologi (30%)	7,5		7.3
d. Kelengkapan unsur dan kualitas penerbit (30%)	7,5		7.2
Total = (100%)			
Nilai Pengusul =	25		24.3

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1. **Kesesuaian dan kelengkapan unsur isi jurnal:**
   Unsur jurnal standar IEEE. Telah ditulis dengan baik.
2. **Ruang lingkup dan kedalaman pembahasan:**
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3. **Kecukupan dan kemutakhiran data/informasi dan metodologi:**
   Referensi masih kurang mutakhir pada saat paper tersebut terbit. Metoda standard dan dapat diverifikasi.
4. **Kelengkapan unsur dan kualitas terbitan:**
   Paper berasal dari konferensi terindeks, nilai max 25

$N = 60\% \times 24.3$
$= 14.58$

Semarang, 10 Feb 2020
Reviewer 1

Prof. Dr. Muhammad Nur, DEA
NIP. 195711261990011001
Bidang ilmu/Unit kerja : Fisika FSM UNDIP

* dinilai oleh dua Reviewer secara terpisah
**coret yang tidak perlu

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		d. Penerbit/Organiser : IEEE
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Kategori Publikasi Jurnal Ilmiah (beri ✓ pada kategori yang tepat) :
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Hasil Penilaian *Peer Review* :

Komponen Yang Dinilai	Nilai Maksimal *Prosiding* Internasional [√]	Nilai Maksimal *Prosiding* Nasional [ ]	Nilai Akhir Yang Diperoleh
e. Kelengkapan unsur isi buku (10%)	2,5		2,5
f. Ruang lingkup dan kedalaman pembahasan (30%)	7,5		7,2
g. Kecukupan dan kemutahiran data/informasi dan metodologi (30%)	7,5		7
h. Kelengkapan unsur dan kualitas penerbit (30%)	7,5		7,5
Total = (100%)			
Nilai Pengusul =	25		24,2

Catatan Penilaian artikel oleh Reviewer :

1. **Kesesuaian dan kelengkapan unsur isi jurnal:** Artikel telah di susun sesuai kaidah ilmiah dan sesuai template dari IEEE proceeding.
2. **Ruang lingkup dan kedalaman pembahasan:** bersifat kuantitatif, lingkup pembahasan mayoritas pembahasan dengan data artikel. Nilai kuantitatif perlu dibahas lebih mendalam terhadap apa yang dilakukan
3. **Kecukupan dan kemutakhiran data/informasi dan metodologi:** Artikel telah disusun dg baik. metode penelitian jelas dan baik. Referensi terkini 5/11 x 100%,
4. **Kelengkapan unsur dan kualitas terbitan:** Artikel terindeks Scopus dan IEEE. Kualitas terbitan baik dan lengkap.

Semarang, 30 - 1 - 2020
Reviewer 2

Prof. Dr. Heri Sutanto, MSi
NIP. 197502151998021001
Bidang ilmu/Unit kerja : Fisika FSM UNDIP

* dinilai oleh dua Reviewer secara terpisah
**coret yang tidak perlu

LEMBAR
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Nama/Jumlah Penulis	:	**Jatmiko E. Suseno**, Munawar A. Riyadi, dan Razali Ismail (3)		
Status Pengusul	:	Penulis pertama/~~penulis ke.....~~ /~~penulis korespondensi **~~		
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		e. Alamat repository PT/web prosiding	:	https://ieeexplore.ieee.org/document/4770370
		f. Terindeks di (jika ada)	:	Scopus

Kategori Publikasi Jurnal Ilmiah (beri ✓pada kategori yang tepat) : [√] *Prosiding* Forum Ilmiah Internasional
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Hasil Penilaian *Peer Review* :

Komponen Yang Dinilai	Nilai Reviewer		Nilai Rata-rata
	Reviewer I	Reviewer II	
a. Kelengkapan unsur isi buku (10%)	2.5	2,5	
b. Ruang lingkup dan kedalaman pembahasan (30%)	7.3	7,2	
c. Kecukupan dan kemutahiran data/informasi dan metodologi (30%)	7.3	7	
d. Kelengkapan unsur dan kualitas penerbit (30%)	7.2	7,5	
Total = (100%)	24,3	24,2	
Nilai untuk Pengusul :			

Semarang, 2020

Reviewer 1

Prof. Dr. Muhammad Nur, DEA
NIP. 195711261990011001
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Prof. Dr. Heri Sutanto, M.Si.
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Document details

IEEE International Conference on Semiconductor Electronics, Proceedings, ICSE
2008, Article number 4770370, Pages 487-490
2008 IEEE International Conference on Semiconductor Electronics, ICSE 2008; Johor Bahru, Johor; Malaysia; 25 November 2008 through 27 November 2008; Category numberCFP08421; Code 76092

Short channel effect of SOI vertical sidewall MOSFET (Conference Paper)

Suseno, J.E.[a,b], Riyadi, M.A.[a,c], Ismail, R.[a]

[a]Faculty of Electrical Engineering, Universiti Teknologi, Malaysia 81310 Skudai, Johor, Malaysia
[b]Physics Department, Diponegoro University, Semarang, 50271, Indonesia
[c]Department of Electrical Engineering, Diponegoro University, Semarang, 50271, Indonesia

Abstract

View references (10)

Application of asymmetric sidewall vertical metal oxide semiconductor field effect transistors (MOSFETs) is hindered by the parasitic overlap capacitance associated with their layout, which is considerably larger than for a lateral MOSFET on the same technology node. A simple process simulation has been developed to reduce the parasitic overlap capacitance in the asymmetric sidewalls vertical MOSFETs by using SOI (Silicon on Insulator) in bottom planar surfaces side. The result shows that while channel length decreases, the threshold voltage goes lower, the DIBL rises and subthreshold swing tends to decrease, for both structures. It is noted that the SVS MOSFET structure generally have better performance in SCE control compared to bulk vertical MOSFET. The presence of buried oxide is believed to increase the performance of vertical MOSFET, essentially in controlling the depletion in subthreshold voltage. © 2008 IEEE.

SciVal Topic Prominence

Topic: MOSFET | Transconductance | Gates

Prominence percentile: 55.159

Author keywords

Parasitic capacitance | Sidewall | SOI | Vertical MOSFETs

Indexed keywords

Engineering uncontrolled terms: Buried oxides | Channel length | Metal-oxide-semiconductor field-effect transistor | MOS-FET | MOSFET structures | Overlap capacitance | Parasitic capacitance | Planar surface | Process simulations | Short-channel effect | Sidewall | Silicon on insulator | SOI | Subthreshold | Subthreshold swing | Technology nodes | Vertical MOSFET | Vertical MOSFETs

Engineering controlled terms: Capacitance | Charge coupled devices | Field effect transistors | Metallic compounds | MOS devices | Semiconducting silicon compounds | Threshold voltage

Engineering main heading: MOSFET devices

ISBN: 978-142442561-7
DOI: 10.1109/SMELEC.2008.4770370
Source Type: Conference Proceeding
Document Type: Conference Paper
Original language: English

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Message From ICSE2008 Conference Chair

I would like to welcome all participants and paper presenters to the 2008 IEEE International Conference on Semiconductor Electronics (ICSE2008) held from 25th to 27th November 2008. I hope you will enjoy the conference technical and social programs as well as the beautiful city of Johor Bahru, Johor, Malaysia, situated at the south of the peninsular and at the boundary of our neighboring country, Singapore.

This is the eighth ICSE organized by the Electron Devices Chapter of IEEE Malaysia Section and technically co-sponsored by Electron Devices Society. Over the last sixteen years, the ICSE has become the preeminent international forum on semiconductor electronics embracing all aspects of the semiconductor technology from circuit device, modeling and simulation, photonics and sensor technology, MEMs technology, process and fabrication, packaging technology and manufacturing, failure analysis and reliability, material and devices and nanoelectronics.

This year's conference consists of more than 170 technical papers and several keynote speeches by four very prominent members of the micro- and nanoelectronics community. Prof Cary Y Yang, from the Center for Nanostructures, Santa Clara, USA will speak on *Carbon-based electrical interconnect and thermal interface material.* Prof Cary Y Yang is a Fellow of the IEEE and a past EDS senior president. The second keynote speaker is Prof Vijay K Arora from the Division of Engineering and Physics at Wilkes University, USA. He will talk on *Quantum Nanoelectronics*. The other two invited speakers are Assoc. Prof. Chim WK from the National University of Singapore who will speak on *Germanium Nanostructures* and Prof John P R David from the University of Sheffield, UK who will be giving us insights into *InGaAsN for optoelectronic applications*.

This year, we have separated the technical program into eight group sessions allowing participants to select the topical area of their choice. I wish all of you a pleasant stay in this country and we hope your attendance in this conference will prove to be an enriching experience.

I would like to express my gratitude to Universiti Kebangsaan Malaysia and Universiti Teknologi Malaysia for their co-operation. I would also like to thank the editorial staff, members of the organizing committee, secretarial staff, and everybody who have worked tirelessly to make this conference a reality and a success.

Thank You.

Prof. Dr. Sahbudin Shaari
Chair, ED Malaysia Chapter
ICSE2008 Conference Chairman

IEEE International Conference on Semiconductor Electronics (ICSE)

2008 IEEE International Conference on Semiconductor Electronics

DOI: 10.1109/icse14162.2008

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Semiconductor Electronics (ICSE), 2008 IEEE International Conference on

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☐ **A case study of NMOS AC hot carrier injection lifetime improvement**
Zhang Dong;David Kho Ching Tien;Koo Sang Sool;Kim Eui Choong
Publication Year: 2008,Page(s):455 - 457
▸ Abstract (html) (1040 Kb) ©

☐ **On the subthreshold measurements of SIC MOSFETs**
Idrees S. Al-Kofahi
Publication Year: 2008,Page(s):458 - 461
▸ Abstract (html) (874 Kb) ©

☐ **Design of 900MHz voltage-controlled oscillator using 0.18μm CMOS technology**
M.H. Siti Maisurah;A. Marzuki;I. Mohd Azmi;A.I. Abdul Rahim;Y. Mohamed Razman
Publication Year: 2008,Page(s):462 - 465
▸ Abstract (html) (1043 Kb) ©

☐ **Performance of the forward-biased RF-LNA with deep n-well NMOS transistor**
S. F. Wan Muhamad Hatta;N. Soin
Publication Year: 2008,Page(s):466 - 469
Cited by: Papers (1)
▸ Abstract (html) (1004 Kb) ©

☐ **Ballistic carrier transport in a quasi-two-dimensional nanoscale field effect transistor (FET)**
Ismail Saad;M. Taghi Ahmadi;Razali Ismail;Vijay K. Arora
Publication Year: 2008,Page(s):470 - 474
▸ Abstract (html) (2426 Kb) ©

☐ **Silicon pillar thickness effect on vertical double gate MOSFET (VDGM) with oblique rotating implantation (ORI) method**
Munawar A. Riyadi;Ismail Saad;Razali Ismail
Publication Year: 2008,Page(s):475 - 479
Cited by: Papers (2)
▸ Abstract (html) (1186 Kb) ©

☐ **Comparison Between OTCP and C-V Extraction Methods for Radiation-Induced Traps in MOSFET Devices**
Hakim Tahi;Boualem Djezzar;Arezki Mokrani;Slimane Oussalah;Abderrazak Smatti;Madjid Benabdelmoumen;Rabah Yefsah;Mohamed Mehlous;Belkacem Mansouri
Publication Year: 2008,Page(s):480 - 483
Cited by: Papers (1)
▸ Abstract (html) (994 Kb) ©

☐ **Improved series resistance model for CMOS ESD diodes**
Norliza binti Kamal;Albert Victor Kordesch;Ibrahim bin Ahmad
Publication Year: 2008,Page(s):484 - 486
Cited by: Papers (1)
▸ Abstract (html) (865 Kb) ©

☐ **Short channel effect of SOI vertical sidewall MOSFET**
Jatmiko E. Suseno;Munawar A. Riyadi;Razali Ismail
Publication Year: 2008,Page(s):487 - 490
Cited by: Papers (1) | Patents (2)
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☐ **Surface morphology of Ni-Fe thin films grown on copper substrates using pulse electrodeposition in ultrasonic field**
R. Balachandran;H.K. Yow;B.H. Ong;R.M. Manickam;K. Anuar;W.T. Teoh;K.B. Tan
Publication Year: 2008,Page(s):491 - 494
▸ Abstract (html) (1949 Kb) ©

☐ **A novel Partial SOI power device with step in buried oxide for improvement of breakdown voltage**
Sharbati Samaneh;Orouji Ali Asghar;Fathipour Morteza
Publication Year: 2008,Page(s):495 - 497
▸ Abstract (html) (935 Kb) ©

Quantum nanoelectronics: Challenges and opportunities

Publisher: IEEE

Cite This

PDF

Vijay K. Arora; Michael L. P. Tan **All Authors**

Abstract:
After forty years of advances in integrated circuit technology, the scaling of Silicon Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has entered the nanometer dimension with the introduction of 90 nm high volume manufacturing in 2004. Presently at 45 nm going to 32 nm node in 2009, the latest technological advancement has led to low power, high-density and high-speed generation of microprocessors. VLSI circuit and device simulation programs rely heavily on the laws of physics that are being discovered and re-discovered as devices are being scaled down to nanometer regime. The scaling of the Si MOSFET below 22 nm may soon meet its fundamental physical limitations. Nevertheless, novel devices and structures such as graphene, carbon nanotube field effect transistors (CNFETs) and nanowires offer a solution to overcome the performance limits. A clear understanding of a unique electronics and transport properties is vital as simulation programs always lag behind in implementing new findings and parameters that may or may not be physics-based. This paper examines quantum and nonohmic transport phenomena that are capable of predicting the performance of a nanostructure in device and circuit simulations. The ideas presented will allow researchers to identify the input physical processes to form an intelligent perspective in interpreting the output obtained.

Published in: 2008 IEEE International Conference on Semiconductor Electronics

Date of Conference: 25-27 Nov. 2008

INSPEC Accession Number: 10428965

Date Added to IEEE *Xplore*: 02 February 2009

DOI: 10.1109/SMELEC.2008.4770261

ISBN Information:

Publisher: IEEE

Conference Location: Johor Bahru, Malaysia

I. Introduction

Quantum effects come into play when device length in one or more of the three Cartesian directions is below the carrier de Broglie wavelength, λ_{dB}. The result is transformation of 3D (bulk) analog-like energy spectrum to a digital one resulting in reduced analog-like dimensionality. The digital nature of the energy spectrum for quantum-confined carriers transforms the density of quantum (digital) states and hence affects the carrier transport, including Ohm's law. Nonohmic transport arises due to the fact that Ohm's law-a linear current-voltage paradigm-on which physicists and electronic circuit designers base their investigations breaks down as devices are scaled down to nanometer scale. In a macro-device of the twentieth century (al voltage for triggering the nonohmic behavior, $V_c = (V_t/$ mperature thermal voltage $V_t = k_B T/q = 26\text{mV}$ and a typical ohmic mean free path $\ell_o = 100\text{nm}$. In these macro- circuits, a 5-V logic voltage was well within the ohmic regime $(\text{V} < \text{V}_\text{c})$. However, as we begin the twenty-first century, a typical device size, L, is in sub-100-nm regime and going smaller, with a critical voltage of 0.26 V or lower. In a micro/nano-circuit, even a low logic voltage of 1 V is above the critical voltage $(\text{V} > \text{V}_\text{c})$. It is a misnomer for one to note

Authors

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Faculty of Electrical Engineering, Universiti Teknologi Malaysia, Skudai, Johor, Malaysia

Carbon-based electrical interconnect and thermal interface materials

Publisher: IEEE

Cite This

PDF

Cary Y. Yang All Authors

Abstract:
Summary form only given. As integrated circuit (IC) technology continues the trend towards sub-45 nanometer feature sizes, it is imperative to retain performance of back-end features such as on-chip interconnects while gaining the cost benefit of scaling. Some major barriers to achieving continuous downward scaling include high resistance and questionable reliability of nanoscale copper lines, and power dissipation in densely packed integrated circuits. This work presents fundamental electrical and thermal characterization of carbon nanofibers (CNF) as a possible solution for next-generation back-end integrated circuit processing. Results of temperature-dependent electrical resistance measurements for CNF arrays demonstrate distinct metallic behavior of these novel nanoscale devices. The current capacity of CNF interconnect test structures is examined and the results are compared with an electrothermal transport model. The use of CNF/copper composite material as a thermal interface for IC packaging is explored and fundamental thermal resistance measurement results show promise of such a composite material for thermal management applications.

Published in: 2008 IEEE International Conference on Semiconductor Electronics

Date of Conference: 25-27 Nov. 2008

INSPEC Accession Number: 10467974

Date Added to IEEE *Xplore*: 02 February 2009

DOI: 10.1109/SMELEC.2008.4770264

ISBN Information:

Publisher: IEEE

Conference Location: Johor Bahru, Malaysia

Authors

Cary Y. Yang
Center for Nanostructures, Santa Clara University, USA

Low noise avalanche photodiodes

Publisher: IEEE

J.P.R. David **All Authors**

Abstract:
Avalanche photodiodes (APDs) are used in many applications when conventional unit y gain photodiodes cannot provide enough sensitivity and the extra amplification provided by the impact ionization process gives it an advantage. Unfortunately this amplification or gain of the incoming optical signal is always accompanied by some 'excess noise' due to the stochastic nature of the ionization process and sets a limit to the maximum useful gain.

Published in: 2008 IEEE International Conference on Semiconductor Electronics

Date of Conference: 25-27 Nov. 2008

INSPEC Accession Number: 10467973

Date Added to IEEE *Xplore*: 02 February 2009

DOI: 10.1109/SMELEC.2008.4770263

ISBN Information:

Publisher: IEEE

Conference Location: Johor Bahru, Malaysia

Avalanche p hotodiodes (APDs) are used in many applications when conventional unit y gain photodiodes cannot provide enough sensitivity and the extra amplification provided by the impact ionization process gives it an advantage. Unfortunately this amplification or gain of the incoming optical signal is always accompanied by some 'excess noise' due to the stochastic nature of the ionization process and sets a limit to the maximum useful gain. Early work by McIntyre showed that the excess noise depended on the ratio of hole ionization coefficient (β) to elec and β are sem iconductor material dependent and unfortu $\approx \beta$, giving rise to relatively high excess noise. In recent years, work done at the University of Sheffield h as shown th at low excess noise can be obtained in hom ojunction structures simply by utilising thin avalanching regions. Experimental results show that contrary to conventional theory, the excess noise actually decreases as the avalanching width reduces. The reason

Authors

J.P.R. David
University of Sheffield, UK

Germanium nanostructures for electronic memory application

Publisher: IEEE

Cite This

PDF

W. K. Chim All Authors

Abstract:
The increasing use of portable electronics and embedded systems has resulted in the need for low-voltage, high-density nonvolatile memory devices. Nanocrystal memories, utilizing the Coulomb blockade effect, have the potential to satisfy such a requirement. The primary motivation in the use of nanocrystal memories is the potential to scale the tunnel dielectric thickness to a small dimension, resulting in lower program and erase voltages during operation. By using nanocrystal charge storage sites that are electrically isolated, charge leakage through localized oxide defects can be reduced, even with the use of a thin tunnel dielectric. In this presentation, methods of synthesizing and controlling the size and distribution of germanium (Ge) nanocrystals in a tri-layer insulator gate stack memory device will be presented. Investigations into the charge storage mechanism and electrical performance of Ge nanocrystal memory devices will be discussed. The role of traps/defects in Ge nanocrystal charge storage and how the energy location of trap levels can be engineered for improved device performance will be presented. Finally, scanning capacitance microscopy/spectroscopy (SCM/SCS), a nanocharacterization technique based on scanning probe microscopy which can be used to analyze electron and hole charging in Ge nanodots, will also be discussed.

Published in: 2008 IEEE International Conference on Semiconductor Electronics

Date of Conference: 25-27 Nov. 2008

INSPEC Accession Number: 10428966

Date Added to IEEE *Xplore*: 02 February 2009

DOI: 10.1109/SMELEC.2008.4770262

ISBN Information:

Publisher: IEEE

Conference Location: Johor Bahru, Malaysia

I. Introduction

Nanostructures have received increasing interest because of their peculiar and superior properties as compared to bulk structures. Nanocrystals, also known as quantum dots, nanodots or artificial atoms, are zero-dimensional structures (as size quantization takes place in three spatial dimensions) typically between 1 and 100 nm. Nanocrystals could potentially be incorporated into charge storage devices and transistors for electronic applications. This is especially useful in device miniaturization to extend the

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