

LEMBAR
HASIL PENILAIAN SEJAWAT SEBIDANG ATAU PEER REVIEW
KARYA ILMIAH : JURNAL ILMIAH

Judul Jurnal Ilmiah (Artikel) : The Effect of Organic Content on Durability and Unconfined Compressive Strength Test of Clay Shale in Bawen, Semarang
 Jumlah Penulis : 4 orang (**Bambang Pardoyo**, Kresno Wikan Sadono, Abdul Haris Baihaqi dan Septiawan Pambudi)
 Status Pengusul : Penulis ke-1
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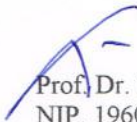
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Vibro-Acoustic Signal Based Fault Diagnosis of Electric Motor Using Artificial Neural Network

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Abstract

This work presents a model for fault detection of an electrical motor using vibration and noise signals. Most of the motor faults generate specific patterns in the motor noise and vibration that can be captured and analyzed for diagnosis. Early detection of motor faults will save the motor from sequent deteriorations into a lot of severe conditions, and thus can save lot of maintenance costs. An accelerometer was used to capture decently accurate information of the motor-vibration and Microphone was used to capture decently accurate information of the noise. Features were extracted in time and frequency domain using which an Artificial Neural Network (ANN) called Multi-Layer Perceptron (MLP) was trained to learn different motor conditions such as healthy and faulty. This study shows that mistreatment easy options and ANN structure will effectively and with efficiency classify differing types of motor faults. The use of low-cost sensors has made this method very attractive to wide range of applications where a cost-effective solution is desired.

Keywords: *Electric motor-Fault Detection, Auto Spectrum, Vibration Analysis, ANN (Artificial Neural Network) and MLP (Multi-Layer Perceptron).*

1. Introduction

A large part of the electrical energy in Egypt is consumed by industries and domestic motors. The manufacturers and consumers of these motors are now interested to include condition-monitoring equipment, by which they can improve the safety and reliability of those equipments. A number of techniques are reported in the literature to diagnose and detect motor faults [1]. Early detection of abnormalities in the motors helps reducing the fault number and associated repair costs. Monitoring the motor condition is important to detect any fault in an early stage that can eliminate the risks of intense motor faults [1].

The influence of vibrations over the system is observed by performing motor current signal analysis to detect the presence of faults. The obtained results show the feasibility of detecting multiple faults in a kinematic chain [2] faults have to be treated before totally damaging the machine and consequently it will reduce the maintenance cost and shutdown time. Thus, there is a growing need for a simple, low cost and reliable technique to detect motor faults. Dejan V. Matijević and Vladimir M [3] studied Modern Contributions in Vehicle Noise and Vibration Refinement with Special Emphasis on Diagnostics. Partha Sarathee et al [1] reviewed faults and fault detection techniques on induction electric motor. Sy-Ruen Huang et al [4] built induction motor fault diagnosis

A Heuristic Technique for Architectural Realization Targeting 3D-Integrated Circuits

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Abstract

A great deal of scaling of CMOS technology over the last three decades has enabled the realization of deep submicron VLSI circuits with billions of transistors on a single silicon chip. However, as minimum feature sizes reach lower than 10 nm, this rapid shrinking of CMOS scaling faces realization challenges associated with semiconductor fabrication, intercommunication delays, power, and energy dissipation. The three-dimensional (3D) approach of VLSI integration circuits (ICs) is a target technology that is used to deal with some of the challenges in the current technology of CMOS-integrated circuits such as number of through-silicon via (TSV) for which, in this paper, we present a heuristic scheme to optimize them. The input of our proposed approach is a data flow graph representing some digital signal processing algorithms that will be stored as list of equations, and the output is a minimized number of TSVs. The proposed scheme targeting 3D VLSI architecture is divided into phases (high-level-syntheses): scheduling, allocation and recourse binding, and layer assignment aimed at optimizing the number of TSV, taking into consideration power per control step in the time schedule. The proposed heuristic scheme is applied to some well-known DSP algorithms and is shown to produce good results compared to those from the conventional approach, in which a very intensive computational time approach (NP-complete), namely, the integer linear programming, is incorporated.

Keywords: *Through-silicon-vias (TSVs), Three-dimensional integration circuits (3D ICs), Data flow graph (DFG), High-level-syntheses (HLS).*

1. Introduction

Over the past century, CMOS-based integrated circuits have faced tremendous growth, and most of today's devices; computers, laptops, smart monitors, and phones, contain a very small transistor component. During that period of time, these components (transistors) have rapidly changed from micro- to nano-scale; the use of electronics has increased while their size has significantly decreased, which brings scope for new ideas and features to be applied in the integrated circuit world where it has previously been impossible due the limited size of digital signal processing chips [1-3]. By the late 1950s, silicon had become the industry's preferred semiconductor material; it replaced the vacuum tubes, which were very low performance devices. By that time, the transistors scale was smaller and much faster according to Moore's law [4]; the number of transistors doubled every one and half years. In fact, thanks to transistors, the size of digital systems changed from the size of the entire room to the size of a human pocket. Transistors cannot keep shrinking forever [5], [6], [7]. As the sizes become smaller; the current integrated circuits more easily leak from the source to the drain through the gain (in the off mode). This will force new ways of thinking and encourage new ideas to arise [7], [8].

With rapid integrated circuit (IC) technology scaling and shrinking to smaller sizes, the complexity of its design and implementation increases with the radical growth of circuits; intercommunication and interconnects technology is lagging such scaling rates, and hence, interconnect delay has increased significantly compared to functional units delay and become a dominant and major source of integrated circuit latency and power

A Secure NFC Transactions via Symmetric Algorithm

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Abstract

Security is an important element for the success of Near Field Communication. Due to high interoperability, protection of NFC data from unauthorized users or attackers are required. NFC provides no reliable security against privacy protection or protection against a device being vulnerable to coincidental reception of malicious data. A few problems such as data modification, data corruption, man in the middle attack and relay attack could be a major threat if any kind of authentication is not involved before the NFC transactions. Hence, implementation of NFC application must consider all possible features which is not only efficiency element, but also secure element is more than necessary to make the fullest use of this technology. The proposed system focuses on the protection of the data and verify the originality of mosquito spray product during NFC transactions using a unique key value and symmetric algorithm and trying to secure the transferred data from various possible attacks.

Keywords

Symmetric Algorithm, Near Field Communication (NFC), Wireless Communication

1.0 Introduction

Wireless communication is one of the fastest growing technologies in communication engineering [1]. This communication can be in long distance or short distance. Wireless communications means transceiving information without using any physical medium. Wireless communications are connected without cables covering everywhere [2]. It is much easier and faster to get devices to communicate without cables. A few technologies in wireless technologies such as RFID (tracking application), NFC (contactless application), IrDA (pointing device), GSM (mobile telecom), and Bluetooth (medicine application) have been used in different applications. This paper focuses on contactless application.

Using ANN for Predicting Bearing Capacity of Shallow Foundations

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Abstract

Shallow foundations ensure the stability of the building when acting as a transmission load from the structure to the soil layer. Therefore, the bearing capacity of shallow foundations is an important indicator to determine the stability of the building. However, determining the bearing capacity of shallow foundations is a challenge for geotechnical engineers, and expensive to manipulate. In this investigation, Artificial neural network (ANN) model is used to predict the bearing capacity of shallow foundations. To perform the simulation, 50 experimental data were collected from the literature. The data set consists of 2 groups of input variables (geometric dimensions of foundation, physical properties of soil) and output variables (bearing capacity of foundation). Evaluation of the models was made and compared on training data set (70% data) and testing data set (30% remaining data) by criteria of Pearson's correlation coefficient (R) and root mean square error (RMSE). The results show that the ANN model can accurately predict the bearing capacity of shallow foundations.

Keywords: Shallow foundations, Bearing capacity, Artificial neural network, Backpropagation algorithm.

1. Introduction

The shallow foundations ensure good transmission of forces from the structure to the soil layer. These forces will be transferred to the shallow foundations according to two mechanisms: the first mechanism, the forces will be a distribution along the foundations in the form of a lateral force, the other will be at the point (point resistance). Analysis of the mechanism of load transfer has made it possible to initiate a considerable number of methods for designing shallow foundations, in particular, determining bearing capacity of shallow foundations. Predicting bearing capacity of shallow foundations has been a challenge for geotechnical engineer. Several methods and approaches have been developed to overcome uncertain prediction. These methods include some simplifying assumptions, using empirical approaches regarding foundation/soil interactions and distribution of soil resistance along the foundations, etc.... The bearing capacity of shallow foundation can be determined by the following two main approaches: (i) experimental test including in situ and laboratory (dynamic test or static test); (ii) theoretical models based on static analysis methods and finite elements.

Experimental test requires a qualified person to manipulate and is costly. The bearing capacity up to the lowest point of foundations can't be estimated [1]. Theoretical methods based on static analysis or numerical models. Considerable uncertainties regarding the horizontal coefficient of soil pressures are assumed in the analysis. In general, the bearing capacity theory deals with non-coherent soils, when the soil is heterogeneous, a difficulty will appear concerning the friction