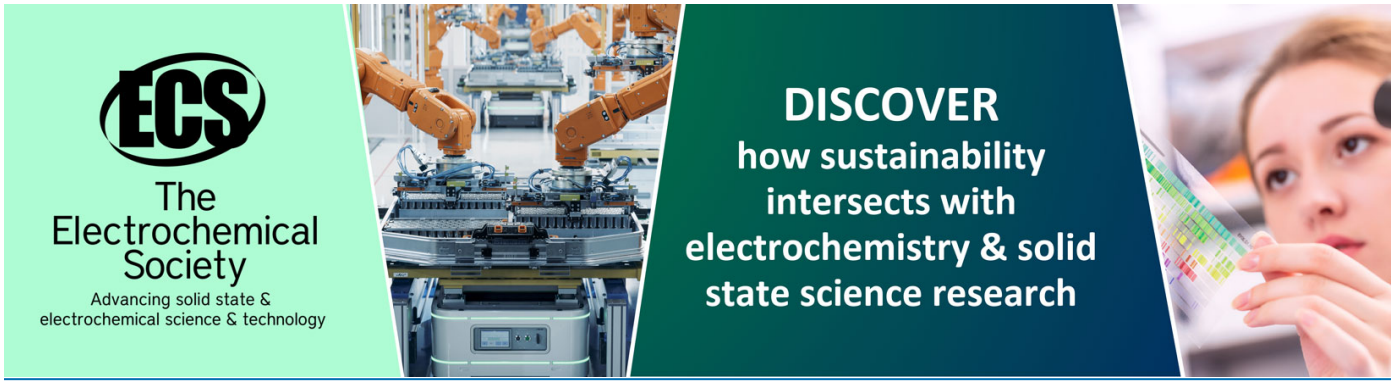
Evaluation and Mitigation of Voltage and Current Unbalance at MSTP Undip Jepara



Evaluation and Mitigation of Voltage and Current Unbalance at MSTP Undip Jepara

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Abstract. Marine Science Techno Park (MSTP) Diponegoro University is a central for the application of technology and research in the fisheries and marine sector under the auspices of Diponegoro University. After measuring the electrical power quality parameters, a voltage and current unbalance problem was found on each SDP and MDP at MSTP Undip Jepara Building. The final project is designed to mitigate current and voltage unbalance with a load equalization method in each phase using ETAP 12.6 software. According to the ANSI C84.1-1995 standard, the maximum current unbalance value is 5% and according to the IEEE 45-2002 standard, the maximum voltage unbalance value is 3%. The equalization results show that the load can decrease the value of current unbalance, voltage unbalance, and neutral current that already meets the standards. Based on the evaluation of existing conditions, the current unbalance value on the MDP decreased from 21.522% to 0.419%, the MDP bus voltage unbalance value decreased from 0.280% to 0.015%, and the neutral current decreased from 35.5 ampere to 1 ampere.

1. Introduction

Marine Science Techno Park (MSTP) Diponegoro University is a central for the application of technology and research in the fisheries and marine sector under the auspices of Diponegoro University. MSTP Undip Jepara has many variations of 1-phase loads such as laptops, LED lights, air conditioners and other laboratory equipment. Installation of loads on buildings that do not consider the amount of active power and total reactive power in each phase can affect electrical power quality problems, namely current and voltage unbalance. The impact of current unbalance causes neutral current to flow in the neutral conductor.

One of the most important factor in consideration of electrical power quality in distribution of electricity in buildings are harmonic distortion and unbalance distortion [1]. Based on previous research by Hossein in 2017 [2], current unbalance and voltage unbalance is a serious problem in the distribution of low-voltage level three-phase systems. In a three-phase system the current unbalance can cause voltage unbalance. Referring to IEEE Std. 45-2002 [3], there is a phenomenon of electric power quality, namely voltage unbalace. The existence of uneven load distribution in a three-phase system triggers a voltage unbalance. Meanwhile, in the ANSI C84.1-1995 standard [4], it is explained that there is a phenomenon of an electric current unbalance with the standards set in it. The existing voltage unbalance can cause current unbalance. Referring to the previous research by Margono in 2021 [5], the analysis of voltage and current unbalance and neutral currents was calculated manually using measurement data. This paper enter the measurement data to ETAP 12.6 software to be simulated and improving the

voltage and current unbalance with load equalization method by moving the 1-phase load until the active power and reactive power in each phase was close to the same.

After measuring using the power quality analyzer at the Undip MSTP, it was found that the current and voltage unbalance values of the building were not following with the standards, in this study a load equalization design will be designed for each phase in a three-phase system at the Undip MSTP Jepara to minimize the magnitude of the voltage and current unbalance according to applicable standards [6]. The maximum voltage unbalance value of the electrical system is 3% which is regulated in IEEE Std. 45-2002, and the maximum current unbalance value of the electrical system is 5% which is regulated in ANSI C84.1-1995.

2. Methodology

2.1. Unbalance Current and Voltage

Voltage unbalance is the maximum deviation from the average value of the three-phase system voltage divided by the average value of the three-phase voltage and expressed as a percentage. Voltage unbalance can also be defined as the ratio of negative or zero sequence components to positive sequence components. [7]. Reffering to [8], "in a three-phase system, voltage unbalance condition is when the phase or line voltage magnitudes are not the same, and the phase angles of each phase varies from the balanced voltage conditions, or both." Experiences in the electrical field as revealed that unequal sharing of single phase loads among the three supply phases, which may also frequently vary is one of the major causes of unbalance [9] Current unbalance is the value of the current flowing in each different phase of the electric power system. In general, current unbalance is caused by uneven load distribution which can be done with load balancing [10].

2.2. Definitions of Unbalance Current and Voltage

There are two definitions of the following current and voltage unbalance:

2.2.1. NEMA Definition. The American Standard ANSI C84.1-1995 defines unbalance as the ratio of the maximum voltage deviation from the average line voltage magnitude to the average line current[4]. Definition of NEMA which known as the line current unbalance ratio (LIUR) can be seen in equation (1).

$$\%\, LIUR = \frac{max\ current\ deviation\ from\ the\ average\ line\ current}{average\ line\ current} \times 100\% \quad (1)$$

According to ANSI Standard C84.1-1995, the current unbalance shall not exceed 5% from the average current in each phase in a three-phase system.

2.2.2. IEEE Definition. The IEEE use the same definition of voltage unbalance as a ANSI C84.1-1995 with current unbalance standard. IEEE Standard 45-2002 defines unbalance as the ratio of the maximum voltage deviation from the average line voltage magnitude to the average line voltage[3]. Definition of IEEE which known as the line current unbalance ratio (LVUR) can be seen in equation (2).

$$\%\, LVUR = \frac{max\ current\ deviation\ from\ the\ average\ line\ voltage}{average\ line\ voltage} \times 100\% \quad (2)$$

According to IEEE Standard 45-2002, the voltage unbalance shall not exceed 3% from the average voltage in each phase in a three-phase system.

2.3. Neutral Current

From the currrent unbalance the occures between the phases, it causes a neutral current which is the resultant current vector beetween the three phase [11]. neutral current can increase the power loss due to the current flowing in the neutral wire. The greater the current imbalance, the greater the power losses in the neutral wire [12].

2.4. System Modelling Before Mitigation

The system is designed on ETAP 12.6 software, several tools are used to simulate load flow analysis and unbalanced load flow analysis and determine neutral current on system [13]. Analysis for the system's unbalance voltage and current will be done using a model of existing system. The system consist of 1 Main Distribution Panel (MDP) which has 3 Sub Distribution Panel (SDP) on each floor. The single line diagram will be shown in Figure 1.

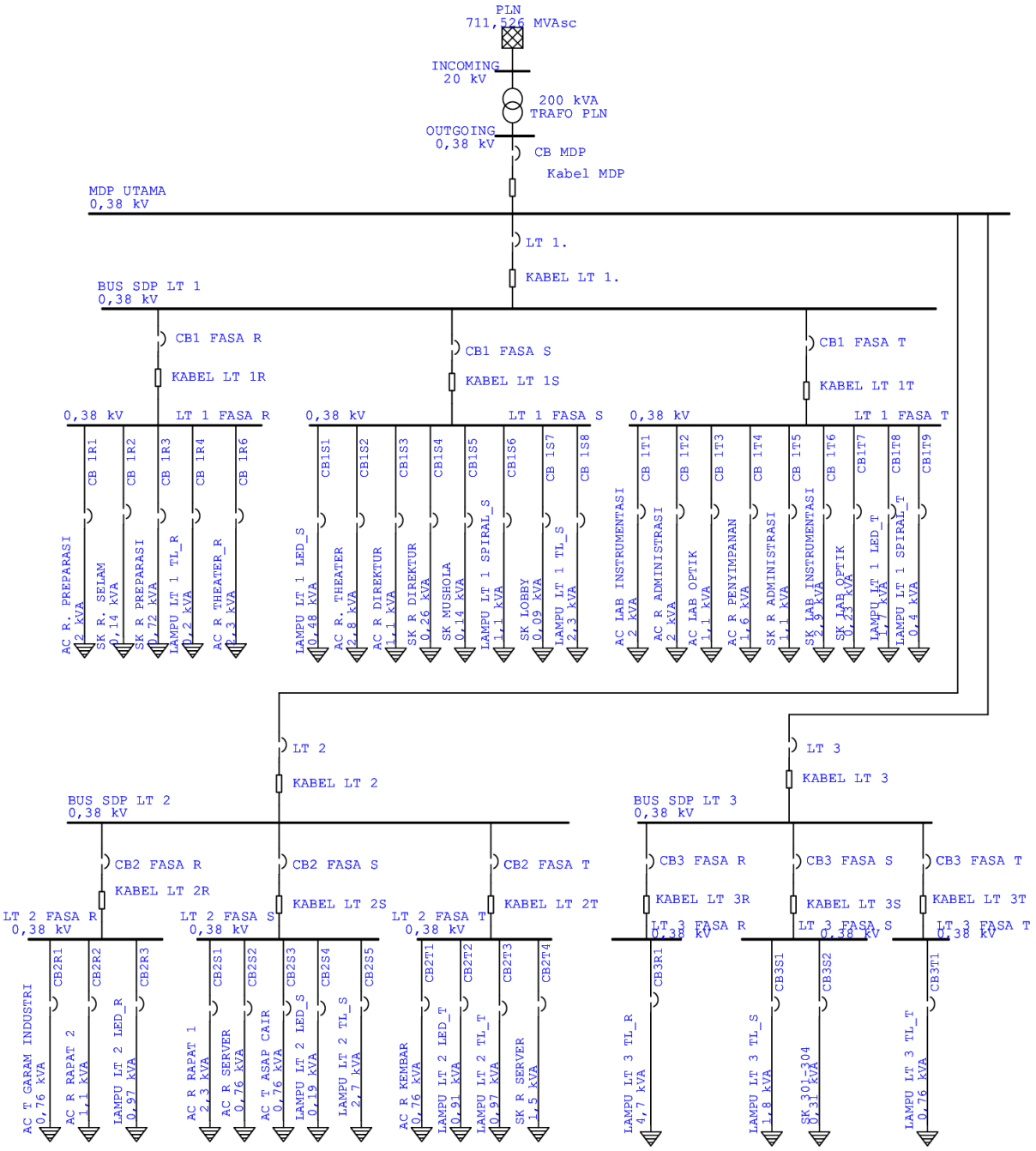

Figure 1. Single line diagram of MSTP Undip Jepara electrical system before mitigation.

2.5. Measurement Result

Measurement were made on 1st Floor SDP panel to 3rd floor SDP panel that connected to the MDP panel. Measurements were carried out using a power quality analyzer on existing conditions. The measured parameters are the current, voltage, power factor, active power and apparent power per phase. The result of measurement are shown in Table 1. An example of the measurement results can be seen in Figure 2.

Table 1. Measurement results of the MSTP Undip Jepara building.

Bus identity	Phase	Current (A)	Voltage (V)	Power factor	Active power (kW)	Apparent power (kVA)
1st Floor	R	23,72	217,9	0,914	4,71	5,15
SDP Bus	S	34,15	217,0	0,852	6,38	7,49
	T	53,16	215,1	0,971	11,36	11,70
2nd Floor	R	11,30	212,5	-0,944	2,37	2,42
SDP Bus	S	28,11	217,8	0,896	5,49	6,12
	T	14,59	218,3	0,936	2,98	3,19
3rd Floor	R	21,60	219,2	0,535	2,50	4,68
SDP Bus	S	9,60	220,7	0,651	1,38	2,12
	T	3,29	224,7	0,535	0,40	0,74

Figure 2. Measurement result of power quality parameter on the 3rd floor SDP panel.

3. Result and Discussion

Based on measurement data and load data, simulation were carried out on ETAP 12.6 software to determine the value of the voltage unbalance, current unbalance and neutral current.

3.1. System Modelling After Mitigation

Single line diagram of MSTP Undip Jepara Electrical System is designed on the ETAP 12.6 software. In order to balance the load, load on the phase with the higher power is transferred to the phase with the lower power until the active power and reactive power are nearly the same. The load equalization results are shown in Figure 3.

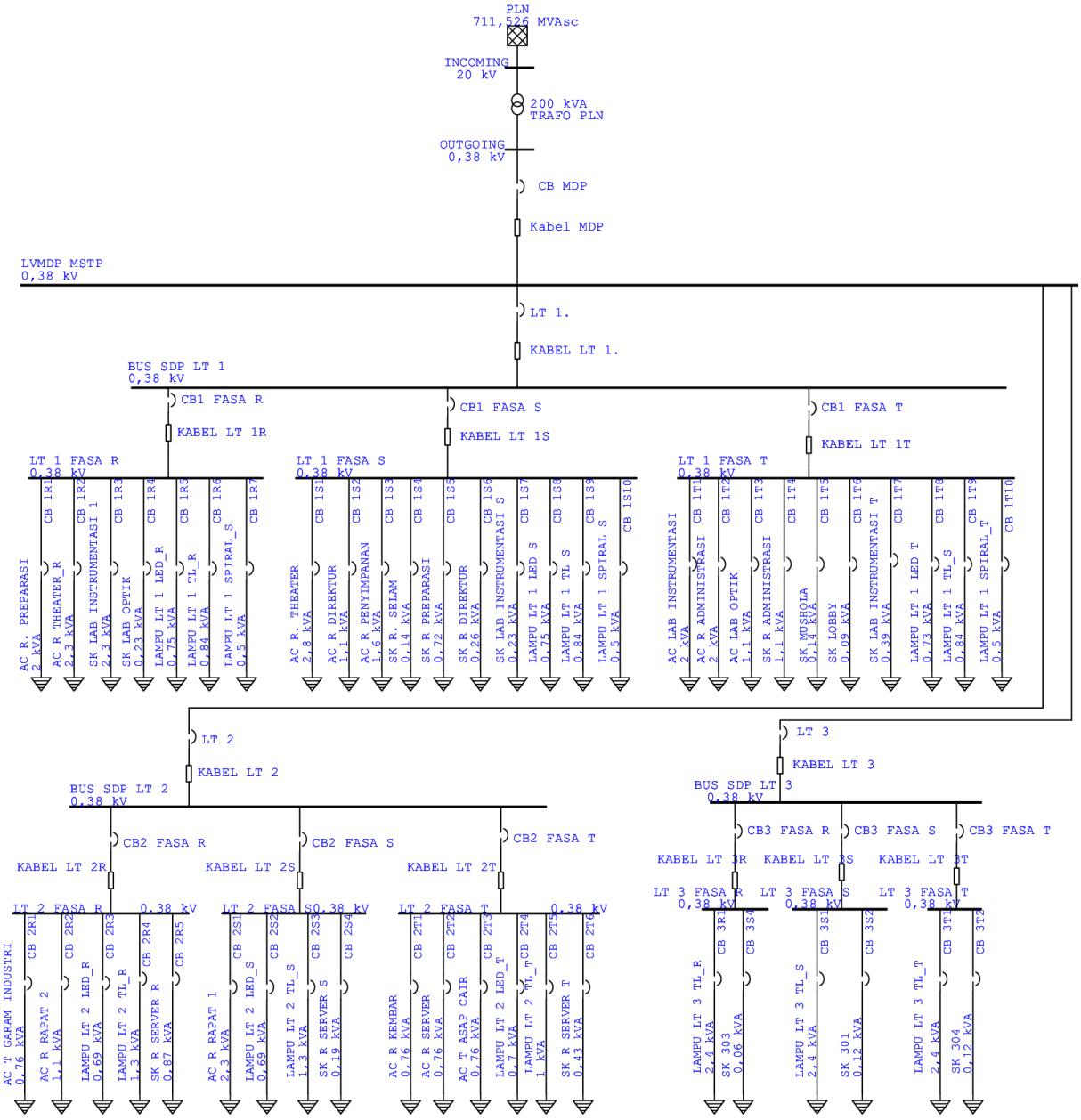

Figure 3. Single line diagram of MSTP Undip Jepara electrical system after mitigation.

3.2. Load Flow Analysis

Based on single line diagram in ETAP 12.6, load flow analysis is carried out to determine the power load flow from the electrical system. The result will be shown on Table 2.

Table 2. Load flow analysis result.

Bus identity	Bus nominal voltage (kV)	Phase	Active power (kW)	Voltage (V)	Current (A)
1st Floor SDP Bus	0,380	R	4,704	217,65	23,7
		S	6,294	216,39	34,1
		T	11,165	216,35	53,2
2nd Floor SDP Bus	0,380	R	2,381	217,91	11,6
		S	5,437	216,49	28,0
		T	2,960	217,06	14,6

3rd Floor SDP Bus	0,380	R	2,524	217,79	21,5
		S	1,374	216,85	9,7
		T	0,408	217,28	3,5
MDP Bus	0,380	R	9,623	218,08	50,2
		S	13,151	217,00	71,3
		T	14,596	217,33	70,4

3.3. Calculation of Voltage and Current Unbalance Before Mitigation

According to IEEE Standard 45-2002, the voltage unbalance shall not exceed 3% from the average voltage in each phase in a three-phase system. Based on equation (1), the voltage unbalance value can be calculated. For the example on 1st floor SDP bus with the voltage data for each phase according to Table 2, the voltage unbalance value is 0,394%.

Based on simulation data result from load flow analysis in Table 2, all SDP and MDP bus voltage unbalance were calculated. All result will be shown in Table 3. According to the result, all voltage unbalance nominal didn't exceed from IEEE Standard 45-2002.

Table 3. Unbalance voltage calculation result.

Bus identity	Voltage (V)			Voltage unbalance (%)
	RN	SN	TN	
1st Floor SDP Bus	217,65	216,39	216,35	0,394
2nd Floor SDP Bus	217,91	216,49	217,06	0,348
3rd Floor SDP Bus	217,79	216,85	217,28	0,222
MDP Bus	218,08	217	217,33	0,280

According to ANSI Standard C84.1-1995, the current unbalance shall not exceed 5% from the average current in each phase in a three-phase system. Based on equation (2), the current unbalance value can be calculated. For the example on 1st floor SDP bus with the current data for each phase according to Table 2, the current unbalance value is 43,784%.

Based on simulation data result from load flow analysis in Table 2, all SDP and MDP bus current unbalance were calculated. All result will be shown in Table 4. According to the result, all current unbalance nominal exceed the ANSI Standard C84.1-1995.

Table 4. Unbalance current calculation result.

Bus identity	Current (A)			Current unbalance (%)
	RN	SN	TN	
1st Floor SDP Bus	23,7	34,1	53,2	43,784
2nd Floor SDP Bus	11,6	28	14,6	54,982
3rd Floor SDP Bus	21,5	9,7	3,5	85,879
MDP Bus	50,2	71,3	70,4	21,522

3.4 Neutral Current Before Mitigation

Using unbalanced Load Flow Analysis in ETAP 12.6, the neutral current are calculated by system. All calculated result will be shown in Table 5.

Table 5. Neutral current result.

Bus identity	Neutral current (A)
1st Floor SDP Bus	34,0
2nd Floor SDP Bus	14,8
3rd Floor SDP Bus	17,2
MDP Bus	35,5

3.5 Comparison of Voltage and Current Unbalance Before and After Mitigation

Due to the current unbalance that exceeds the ANSI C84.1-1995 standard, the load distribution is improved by equalizing the load in each phase until the active power and reactive power in each phase

are close to the same [6]. The results of equalizing the load can reduce the value of the voltage unbalance and current unbalance to meet the standards. The results of the comparison of voltage unbalance can be seen in Table 6. From voltage unbalance data on Table 6, the result are depicted in the graph in Figure 4.

Table 6. Comparison of voltage unbalance before and after mitigation.

Bus identity	Voltage unbalance percent (%)	
	Before	After
1st Floor SDP Bus	0,394	0,015
2nd Floor SDP Bus	0,348	0,015
3rd Floor SDP Bus	0,222	0,015
MDP Bus	0,280	0,015

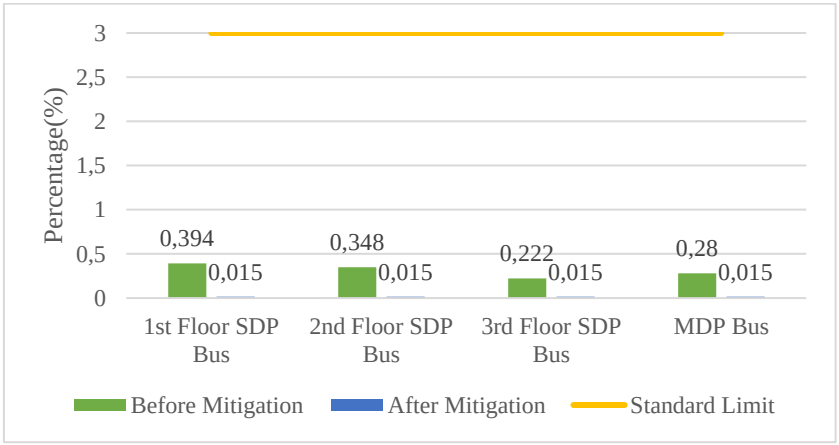

Figure 4. The percentage comparison graph of voltage unbalance before and after mitigation.

The results of the comparison of current unbalance can be seen in Table 7. From current unbalance data on Table 7, the result are depicted in the graph in Figure 5.

Table 7. The percentage comparison of current unbalance before and after mitigation.

Bus identity	Current unbalance percent (%)	
	Before	After
1st Floor SDP Bus	43,784	0,454
2nd Floor SDP Bus	54,982	0,774
3rd Floor SDP Bus	85,879	1,153
MDP Bus	21,522	0,419

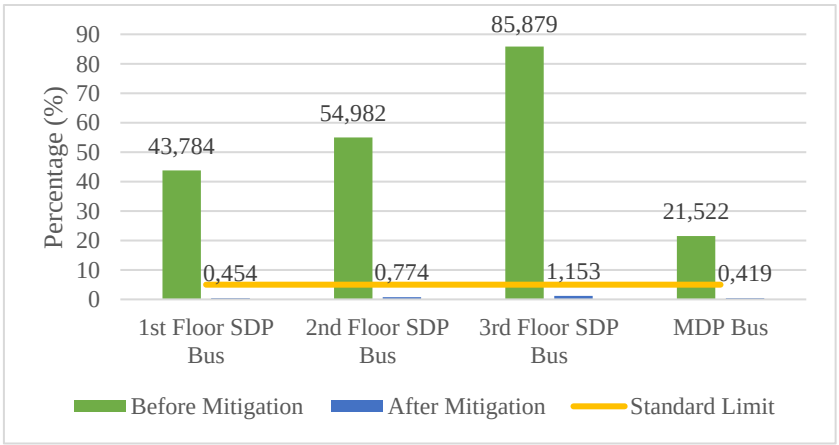

Figure 5. The percentage comparison graph of currrent unbalance before and after mitigation.

3.6. Comparison of Neutral Current Before and After Mitigation

The current unbalance value drops due to load equalization which makes the neutral current decreases. Neutral current will be compared between before mitigation and after mitigation in Table 8, the result are depicted in the graph in Figure 6.

Table 8. Comparison of neutral current before and after mitigation.

Bus identity	Neutral current (A)	
	Before	After
1st Floor SDP Bus	34,0	0,3
2nd Floor SDP Bus	14,8	0,4
3rd Floor SDP Bus	17,2	0,3
MDP Bus	35,5	1,0

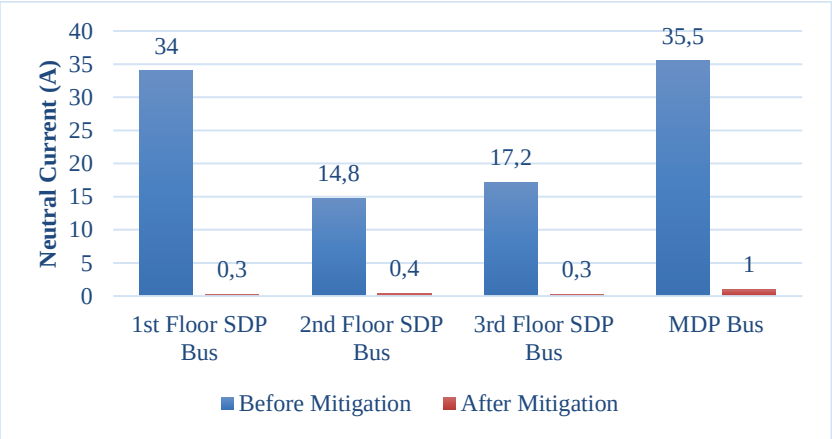

Figure 6. Comparison graph of neutral current before and after mitigation.

4. Conclusion

Based on the evaluation results, the design of unbalance mitigation in the form of equalizing the load in each phase can reduce the current and voltage unbalance values. After mitigation, all buses have an unbalance value below 3% according to the IEEE 45-2002 standard, the current unbalance value is below 5% according to the ANSI C84.1-1995 standard, while the neutral current value and power losses are almost close to zero at each SDP and MDP bus Undip Jepara MSTP Building.

Acknowledgment

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